MT7975DN Datasheet

802.11ax Wi-Fi 2x2 Dual-band Con-current + Bluetooth v5.1 RF Chip

Version: 1.2
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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
V1.0	2019/10/4	Kevin	1.Formal version.
V1.1	2019/11/7	Kevin	1.remove power on sequence.
V1.2	2019/11/13	Kevin	1. correct AVDD18 power pin connection to 1.8V supply. 2. Update the table of contents. 3. Update WRI 9-bit bus interface diagram.

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Lists of Figures and Tables

1 System Overview

1.1 Functional Block Diagram

MT7975DN is an IEEE 802.11ax 2x2 A-band + 2x2 G-band MIMO and Wi-Fi/BT 2-in-1 chip which contains 2.4 GHz WI-Fi transceiver front-ends, 5 GHz Wi-Fi transceiver front-ends, and a Bluetooth transceiver front-end in a DRQFN package. Dedicated Dynamic Frequency Selection (DFS) and Spectrum Monitor (SM) receivers are included to support coexist with 5GHz radar or other 2.4G WIFI systems. Simplified block diagram and how MT7975DN is used are shown in Figure 1-1. The top control logics control each subsystem independently. Each subsystem also has dedicated LDOs. A thermal sensor and a low-speed ADC (Analog-to-Digital Converter) are provided to monitor MT7975DN's temperature variation. MT7975DN have its dedicated crystal oscillator (XO) circuit. Besides, XO circuit provides an external clock source to other chips in the platform.

The transceiver front-ends are on MT7975DN while the ADC/DAC (Analog-to-Digital Converter/Digital-to-Analog Converter) is in the companion modem chip. The interface drivers/receiver buffers are designed to drive PCB trace loading.

Compared to its predecessor MT7615, MT7975DN exhibits the following new features: (1) WiFi 2.4/5GHz support MIMO 11ax (2) Dedicated 5GHz DFS receiver to monitor environment without throughput degradation (3) Dedicated 2.4GHz Spectrum-Monitor (SM) receiver to monitor environment without throughput degradation (4) Dedicated BT front-end for variant application.

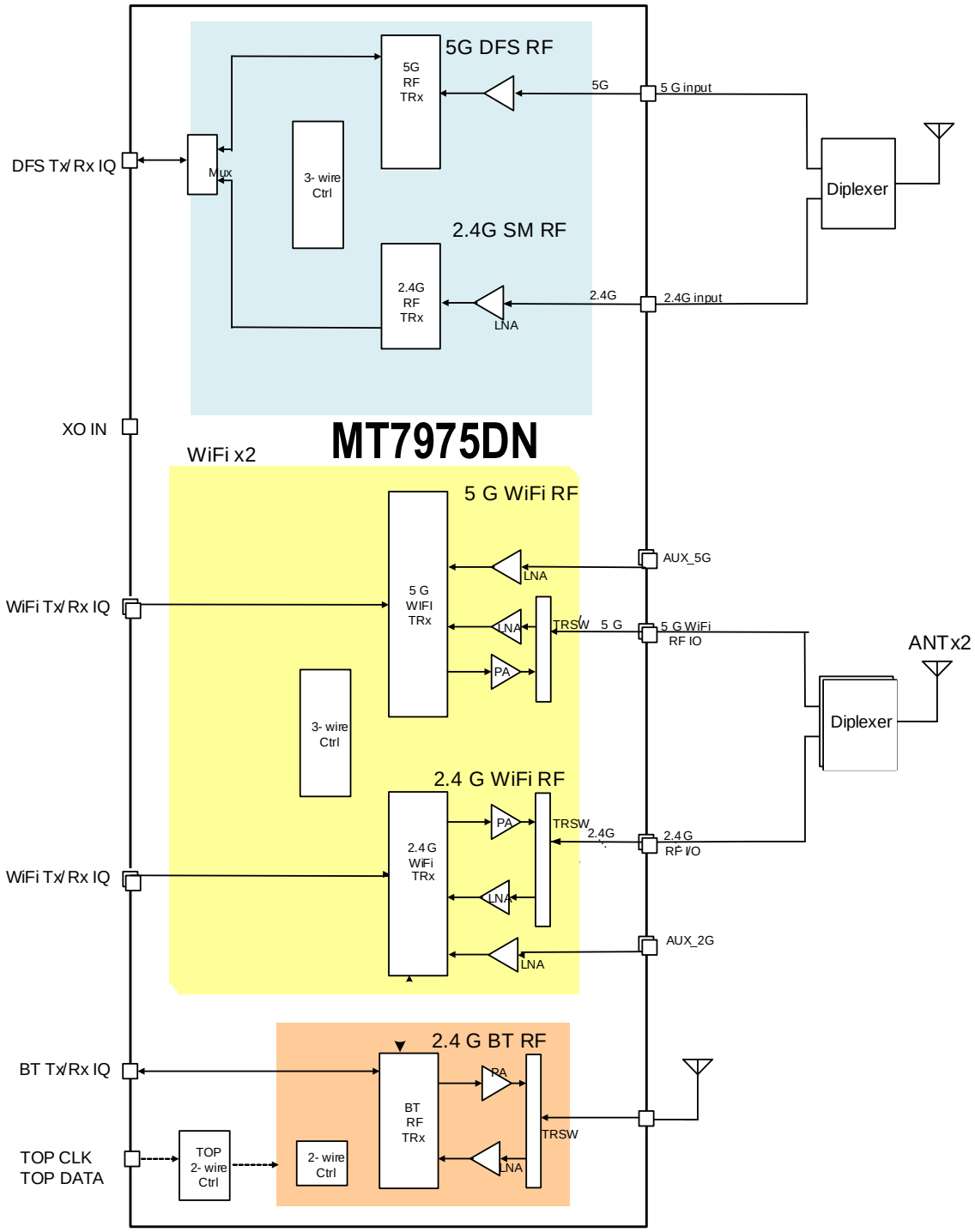


Figure 1-1. MT7975DN block diagram

1.2 Features

- MT7975DN is a 2-in-1 Wi-Fi/BT chip which contains one BT and 2x2 MIMO 2.4/5G GHz Wi-Fi transceiver front-end, including a 5GHz DFS receiver front-end and a 2.4GHz Spectrum-Monitor receiver front-end in a DRQFN package.

1.2.1 Wi-Fi Transceiver

WLAN

- Dual-band (2.4GHz and 5GHz) 2x2 MIMO 802.11 a/b/g/n/ac/ax RF, 20/40/80MHz bandwidth
- Configurable to 2x2 MIMO A-band, or 2x2 MIMO G-band, or 2x2 MIMO A-band+ 2x2 MIMO G-band.
- Supports worldwide Wi-Fi 5G channel including new band in US and China (5925MHz)
- Integrated 2.4GHz/5GHz PA, LNA and TRSW.
- Integrated power detector to support per packet Tx power control
- Built-in calibrations for PVT variation
- Configurable Wi-Fi 2.4/5GHz PA for higher efficiency in low-power applications.
- Supports external PA and LNA for WiFi-2.4GHz and WiFi-5GHz.
- Simultaneous operation (FDD) of 2x2 WiFi-2.4GHz and Bluetooth

1.2.2 Dynamic Frequency Selection Receiver (DFS)

DFS

- Dedicated Zero-Wait Dynamic Frequency Selection (DFS) receiver.
- 5GHz operation frequency.
- Allows wireless LANs to coexist with radar systems.

1.2.3 Bluetooth Transceiver

BT

- Bluetooth specification v2.1+EDR, 3.0+HS, v4.2+HS and v5.1+HS compliant
- Bluetooth 5 dual mode for LE 2Mbps, LE long range, and advertise extension
- Integrated PA
- Low-power scan function to reduce power consumption in scan modes
- Simultaneous operation (FDD) of 2x2 WiFi-5GHz and Bluetooth

2 Pin Definitions

2.1 Pin Layout

MT7975DN uses DRQFN package of with 10.5mm x 9mm dimension.

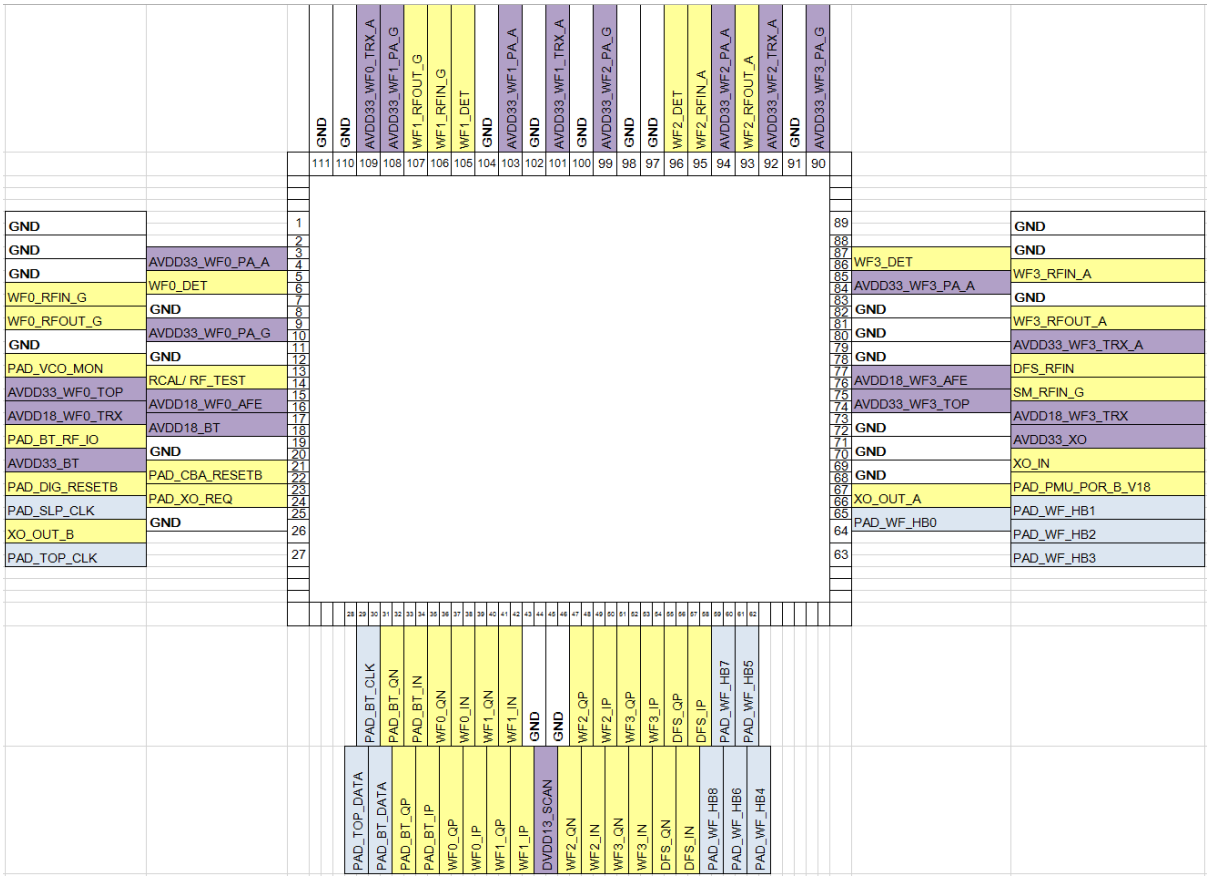


Figure 2-1. MT7975DN pin definition

2.2 IO Definitions

The IO definitions used in Table 2-1 are listed below.

Table 2-1. I/O definitions

Pad attribute	
AI	Analog input (excluding pad circuitry)
AO	Analog output (excluding pad circuitry)
AIO	Analog bidirectional (excluding pad circuitry)
DIO	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
Z	High-impedance (high-Z) output
NP	No internal pull
PU	Internal pull-high
PD	Internal pull-low
ADIO	Analog and digital IO (excluding pad circuitry)
Power	Voltage supply
GND	Ground
NC	No connection

2.3 Pin Definitions

Details pin descriptions of MT7975DN are listed in the following table.

DRQFN	Pin Name	Pin description	PU/PD	I/O	Supply domain
GND pins					
1,2,7,10,11, 19,25,43,45, 69,71,73,79, 81,83,84,91, 100,110,111 ,102,98,89,4 ,104,97,88	GND	GND	N/A	GND	
12	PAD_VCO_MON	GND	N/A	GND	
13	RF_TEST	GND	N/A	GND	
NC pins					
44	NC (DVDD13_SCAN)	Digital LDO output	N/A	NC	
Reset and clocks					
70	XO_IN	Crystal input or external clock input	N/A	AI	
72	AVDD33_XO	XO 3.3v power supply	N/A	Power	
67	XO_OUT_A	XTAL buffered clock output	N/A	AO	
26	XO_OUT_B	XTAL buffered clock output	N/A	AO	
BT interface					
20	AVDD33_BT	RF 3.3v power supply	N/A	Power	
17	AVDD18_BT	RF 1.8v power supply	N/A	Power	
18	PAD_BT_RF_IO	BT RF port	N/A	AIO	
34	PAD_BT_IP	BT IF TRX IQ signals	N/A	AIO	
33	PAD_BT_IN	BT IF TRX IQ signals	N/A	AIO	
32	PAD_BT_QP	BT IF TRX IQ signals	N/A	AIO	
31	PAD_BT_QN	BT IF TRX IQ signals	N/A	AIO	
WIFI Power supply					
14	AVDD33_WF0_TOP	RF 3.3v power supply	N/A	Power	
75	AVDD33_WF3_TOP	RF 3.3v power supply	N/A	Power	
16	AVDD18_WF0_TRX	RF 1.8v power supply	N/A	Power	
74	AVDD18_WF3_TRX	RF 1.8v power supply	N/A	Power	
15	AVDD18_WF0_AFE	RF 1.8v power supply	N/A	Power	
77	AVDD18_WF3_AFE	RF 1.8v power supply	N/A	Power	
109	AVDD33_WF0_TRX_A	RF 3.3v power supply	N/A	Power	
101	AVDD33_WF1_TRX_A	RF 3.3v power supply	N/A	Power	

92	AVDD33_WF2_TRX_A	RF 3.3v power supply	N/A	Power	
80	AVDD33_WF3_TRX_A	RF 3.3v power supply	N/A	Power	
3	AVDD33_WF0_PA_A	RF 3.3v power supply	N/A	Power	
103	AVDD33_WF1_PA_A	RF 3.3v power supply	N/A	Power	
94	AVDD33_WF2_PA_A	RF 3.3v power supply	N/A	Power	
85	AVDD33_WF3_PA_A	RF 3.3v power supply	N/A	Power	
9	AVDD33_WF0_PA_G	RF 3.3v power supply	N/A	Power	
108	AVDD33_WF1_PA_G	RF 3.3v power supply	N/A	Power	
99	AVDD33_WF2_PA_G	RF 3.3v power supply	N/A	Power	
90	AVDD33_WF3_PA_G	RF 3.3v power supply	N/A	Power	
WIFI Radio Frequency interface					
5	WF0_DET	External TSSI DC/AC input	N/A	AI	
105	WF1_DET	External TSSI DC/AC input	N/A	AI	
96	WF2_DET	External TSSI DC/AC input	N/A	AI	
87	WF3_DET	External TSSI DC/AC input	N/A	AI	
93	WF2_RFIO_A	RF A-band RF port	N/A	AIO	
82	WF3_RFIO_A	RF A-band RF port	N/A	AIO	
8	WF0_RFIO_G	RF G-band RF port	N/A	AIO	
107	WF1_RFIO_G	RF G-band RF port	N/A	AIO	
95	WF2_RFIN_A	A-band External LNA input	N/A	AI	
86	WF3_RFIN_A	A-band External LNA input	N/A	AI	
6	WF0_RFIN_G	G-band External LNA input	N/A	AI	
106	WF1_RFIN_G	G-band External LNA input	N/A	AI	
WIFI Analog interface					
38	WF0_IP	WF0 IF TRX IQ signals	N/A	AIO	
37	WF0_IN	WF0 IF TRX IQ signals	N/A	AIO	
36	WF0_QP	WF0 IF TRX IQ signals	N/A	AIO	
35	WF0_QN	WF0 IF TRX IQ signals	N/A	AIO	
42	WF1_IP	WF1 IF TRX IQ signals	N/A	AIO	
41	WF1_IN	WF1 IF TRX IQ signals	N/A	AIO	
40	WF1_QP	WF1 IF TRX IQ signals	N/A	AIO	
39	WF1_QN	WF1 IF TRX IQ signals	N/A	AIO	
49	WF2_IP	WF2 IF TRX IQ signals	N/A	AIO	
48	WF2_IN	WF2 IF TRX IQ signals	N/A	AIO	
47	WF2_QP	WF2 IF TRX IQ signals	N/A	AIO	
46	WF2_QN	WF2 IF TRX IQ signals	N/A	AIO	

53	WF3_IP	WF3 IF TRX IQ signals	N/A	AIO	
52	WF3_IN	WF3 IF TRX IQ signals	N/A	AIO	
51	WF3_QP	WF3 IF TRX IQ signals	N/A	AIO	
50	WF3_QN	WF3 IF TRX IQ signals	N/A	AIO	
DFS/SM interface					
78	DFS_RFIN	DFS RF port	N/A	AI	
76	SM_RFIN_G	SM RF port	N/A	AI	
57	DFS_IP	DFS/SM IF RX IQ signal	N/A	AO	
56	DFS_IN	DFS/SM IF RX IQ signal	N/A	AO	
55	DFS_QP	DFS/SM IF RX IQ signal	N/A	AO	
54	DFS_QN	DFS/SM IF RX IQ signal	N/A	AO	
Digital IOs					
22	PAD_DIG_RESETB	Hardware reset from companion modem	PU/PD	DI	DVDDIO
21	PAD_CBA_RESETB	software reset from companion modem	PU/PD	DI	DVDDIO
23	PAD_XO_REQ	XO enable control from companion modem	PU/PD	DI	DVDDIO
24	PAD_SLP_CLK	Sleep CLK input	PU/PD	DI	DVDDIO
28	TOP_DATA	TOP 2-wire data signal	PU/PD	DIO	DVDDIO
27	TOP_CLK	TOP 2-wire clock signal	PU/PD	DI	DVDDIO
29	BT_CLK	BT 2-wire clock signal	PU/PD	DI	DVDDIO
30	BT_DATA	BT 2-wire data signal	PU/PD	DIO	DVDDIO
58	PAD_WF_WRI8	WF high speed control bus	PU/PD	DIO	DVDDIO
59	PAD_WF_WRI7	WF high speed control bus	PU/PD	DIO	DVDDIO
60	PAD_WF_WRI6	WF high speed control bus	PU/PD	DIO	DVDDIO
61	PAD_WF_WRI5	WF high speed control bus	PU/PD	DIO	DVDDIO
62	PAD_WF_WRI4	WF high speed control bus	PU/PD	DIO	DVDDIO
63	PAD_WF_WRI3	WF high speed control bus	PU/PD	DIO	DVDDIO
64	PAD_WF_WRI2	WF high speed control bus	PU/PD	DIO	DVDDIO
66	PAD_WF_WRI1	WF high speed control bus	PU/PD	DIO	DVDDIO
65	PAD_WF_WRI0	WF high speed control bus	PU/PD	DIO	DVDDIO
68	PAD_PMU_POR_B_V18	Chip enable from companion modem	PU/PD	DI	DVDDIO

Table 2-2 MT7975DN common pin descriptions

3 Electrical Characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD18	1.8V Supply Voltage	-0.3 to 1.89	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V
VESD	ESD protection (CDM)	+/- 250	V

Table 3-1 Absolute maximum rating

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	3	3.3	3.6	V
VDD18	1.8V Supply voltage	1.71	1.8	1.89	V
$T_{JUNCTION}$	Industry junction operating temperature	-20	25	125	°C
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 3-2 Recommended operating range

3.3 Power Supply Specifications

The following tables list the power supply requirements for VDD18 and VDD33.

Table 3-3. AVDD18 specifications

Test item	Min.	Typ.	Max.	Unit	Notes
Output voltage, VDD	1.71	1.8	1.89	V	
Output current				mA	

Table 3-4. AVDD33 specifications

Test Item	Min	Typ	Max	Unit	Notes
Output voltage	3.0	3.3	3.6	V	
Output current				mA	

.

3.4 Digital Logic Characteristics

MT7975DN's timing characteristics and interface protocols are shown here, including some general comments.

3.4.1 Timing Diagram Convention

Figure 3-1 shows the conventions used with timing diagram throughout this document.

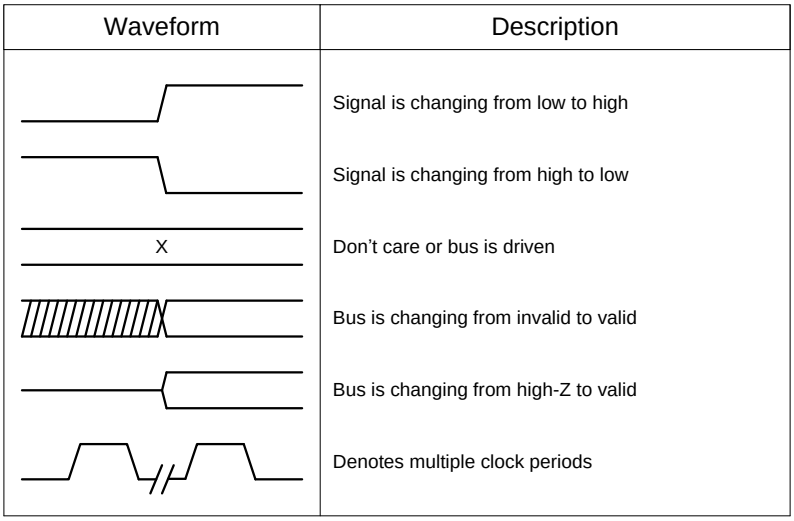


Figure 3-1. Timing diagram conventions

3.4.2 Rising/Falling Time Definition

Figure 3-2 is the rising and falling timing diagram. The actual signal timing curve is related to the external load conditions. See **Error! Reference source not found.** for the operating conditions of digital logics.

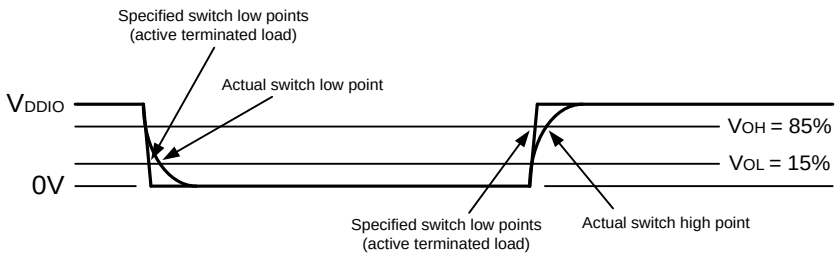


Figure 3-2. Rising and falling times diagram

Table 3-5. Operating conditions of digital logics

Parameter	Min.	Typ.	Max.	Unit	Notes
VDDIO, supply of IO Power	3	3.3	3.6	V	
VIH, input logic high voltage	0.7*VDD		VDD+0.5	V	
VIL, input logic low voltage			0.3*VDDIO	V	
VOH (DC), DC output high voltage	0.7*VDD		VDD+0.5	V	VDD=min, I_{OH}=1.5mA
VOL (DC), DC output low voltage			0.3*VDD	V	VDD=min, I_{OL}=1.5mA

3.4.3 Protocols

There are three main interfaces for MT7975DN:

- 2-wire top control interface: Generally used for all systems (BT/Wi-Fi)
- 9-wire bus: High-speed interface, for Wi-Fi
- 2-wire BT control interface: Dedicated used for BT control

3.4.3.1 2-Wire

The 2-wire bus of MT7975DN is mainly used as below:

- Top control interface, the main interface to access Wi-Fi/BT/TOP command registers
- BT control interface, dedicated used for BT control

The bit number of SDATA depends on different operating conditions, as shown in Figure 3-3.

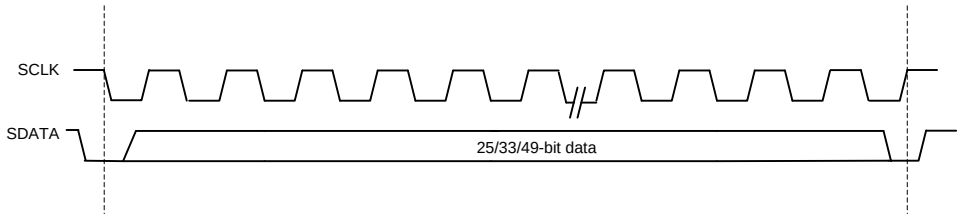


Figure 3-3. 2-wire SPI timing diagram

3.4.3.2 9-bit Bus

MT7975DN has a dedicated 9-bit bus to control the Wi-Fi radio. The related control definitions depend on operating modes and conditions. The protocol is shown in Figure 3-4.

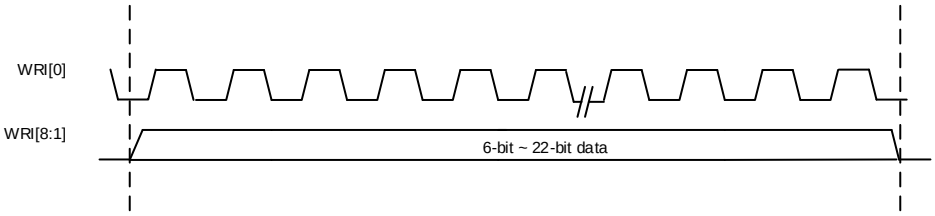


Figure 3-4. Wi-Fi 9-wire SPI access

3.5 MT7975DN TOP Building Blocks

3.5.1 Thermal ADC

A low-speed ADC converts the output of thermal sensor. The temperature coverage range is between -40°C and 120°C. The chip top control may do corresponding adjustment (such as PA/TX gain switching) based on such temperature information.

3.6 Wi-Fi

MT7975DN Wi-Fi is a high performance and highly-integrated dual-band RF transceiver fully compliant with IEEE 802.11 a/ac/ax/b/g/n standards. A novel RF front-end topology is implemented to achieve maximum hardware sharing between 2.4GHz/5GHz Wi-Fi and Bluetooth with integrated TR-switches. MT7975DN also features a self-calibration scheme to compensate the process and temperature variation to maintain high performance. The calibration is performed automatically right after the system boot-up.

3.6.1 2.4GHz Wi-Fi Tx

The 2.4G transmitter utilizes the most cost efficient direct up architecture and integrates a high performance PA with on-chip balun. 2.4GHz WiFi Tx share RFIO port with 2.4GHz WiFi Rx by integrating on-chip T/R switch. The data are digitally modulated in the baseband processor from the companion chip, then up-converted to 2.4GHz RF channels through the DA converter, filter, IQ up-converter and power amplifier.

3.6.2 2.4GHz Wi-Fi Rx

Direct down-conversion receiver architecture is also used in 2.4G Wi-Fi Rx, which consists of a high linearity, low noise figure single-ended LNA with on-chip integrated T/R switch, a quadrature passive mixer and a bandwidth-programmable low-pass filter with DC offset cancellation embedded.

3.6.3 2.4GHz Wi-Fi Sx

A fractional-N frequency synthesizer is implemented to support Wi-Fi LO signal. The frequency synthesizer is capable of supporting various crystal clock frequencies. VCO operates at different freq from RF frequency to avoid any coupling with RF front-end circuitry. An LO generation is employed to divide the VCO signal and generate I/Q quadrature signals.

3.6.4 5GHz Wi-Fi Tx

The 5G transmitter utilizes the most cost efficient direct up architecture and integrates a high performance PA with on-chip balun. The data are digitally modulated in the baseband processor from the companion baseband chip, then up-converted to 5GHz RF channels through the DA converter, low-pass filter, IQ up-converter and power amplifier. The power amplifier is capable of transmitting 22dBm OFDM power.

3.6.5 5GHz Wi-Fi Rx

Direct down-conversion receiver architecture is also used in 5G Wi-Fi Rx, which consists of a high linearity, low noise figure single-ended LNA with on-chip integrated T/R switch, a quadrature passive mixer and a bandwidth-programmable low-pass filter with DC offset cancellation embedded.

3.6.6 5GHz Wi-Fi Sx

A-band Sx adopts LO architecture while VCO frequency is different from RF frequency to avoid TX pulling. Thus, it is composed of PLL, offset LO mixer and a repeater. In MT7975DN application, major Sx supply voltage is 1.8V, and internal cap-less LDO regulates this 1.8V into 1.35V for core circuit operation. Sx generates I/Q quadrature phase to TRX mixer.

4 XO and Bootstrap

4.1 XTAL oscillator

The table below lists the requirement for the XTAL.

Parameter	Value
Frequency	40MHz
Frequency stability	±10 ppm @ 25℃
Operation temperature range	<-40deg , >60deg
ESR	Max <30ohm
CL	10.5p~12.0p
TS	TS min >=10ppm/pF
DL	>=100uW
Dimension	2520

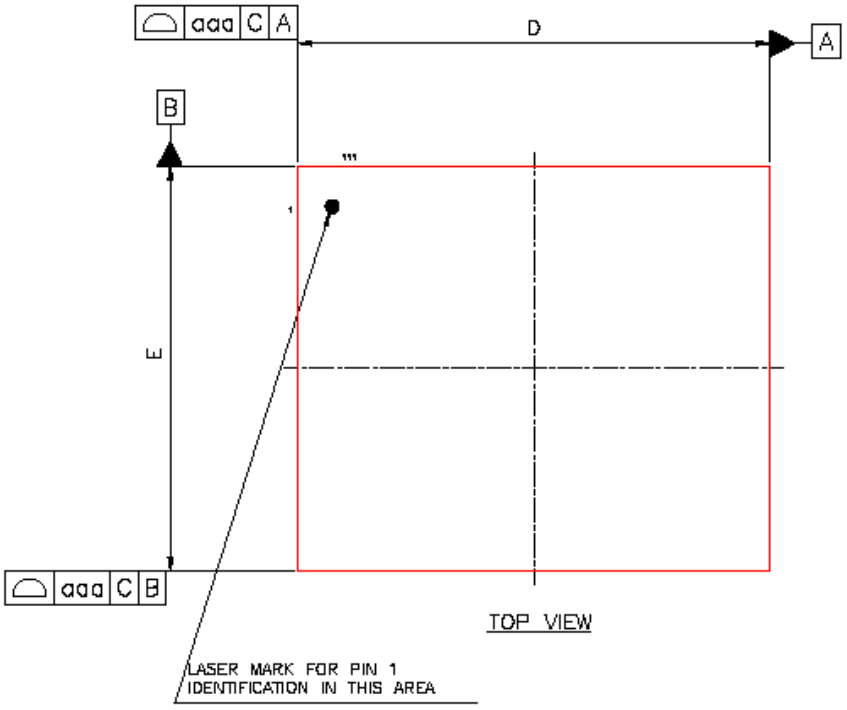
Table 4-1 XTAL oscillator requirement

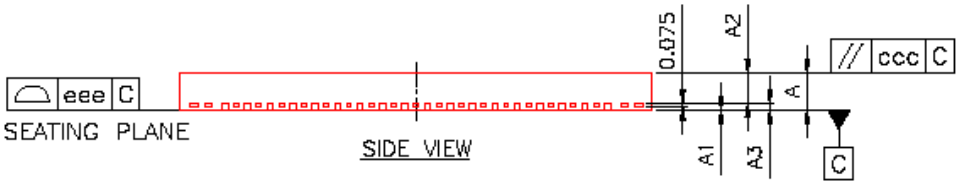
5 Mechanical Information

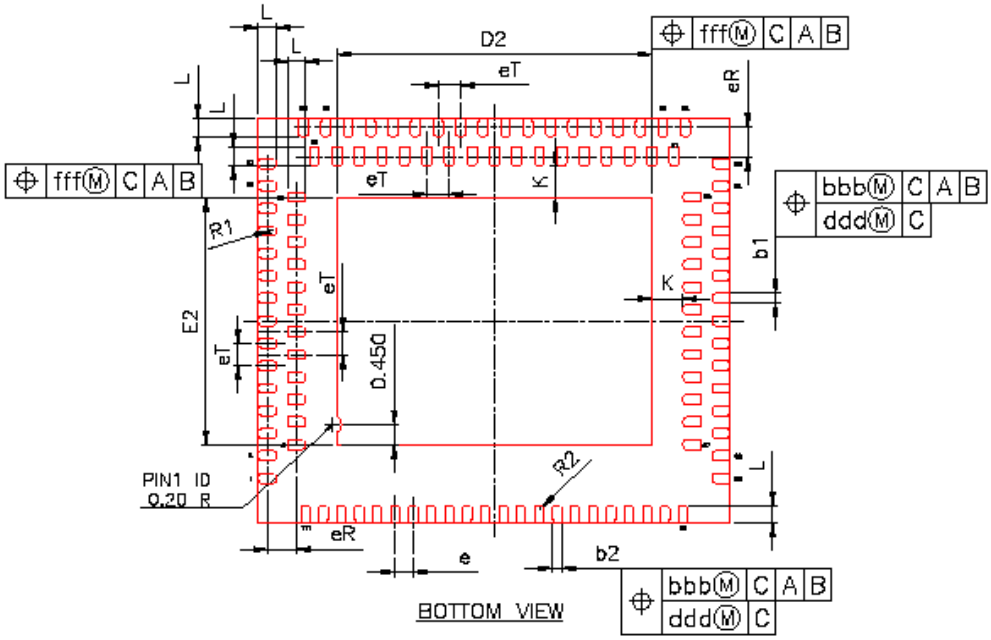
5.1 Device Physical Dimension/Part Number

MT7975DN uses DRQFN package. The physical dimension is shown in Figure 5-1.

Figure 5-1. Physical dimension of MT7975DN







Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.80	0.85	0.90
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.65	0.70	0.75
leadframe thickness		A3	0.15 REF.		
lead width		b1	0.18	0.22	0.30
		b2	0.15	0.20	0.25
package size	X	D	10.4	10.5	10.6
	Y	E	8.90	9.00	9.10
E-PAD size	X	D2	6.90	7.00	7.10
	Y	E2	5.40	5.50	5.60
lead length		L	0.30	0.40	0.50
lead pitch		eT	0.50 bsc		
		e	0.40 bsc		
		eR	0.65 bsc		
lead arc		R1	0.09	---	0.14
		R2	0.075	---	---
Lead to E-PAD tolerance		K	0.20	---	---
Package profile of a surface		aaa	0.10		
Lead position		bbb	0.10		
Parallelism		ccc	0.10		
Lead position		ddd	0.05		
Lead profile of a surface		eee	0.08		
Epad position		fff	0.10		

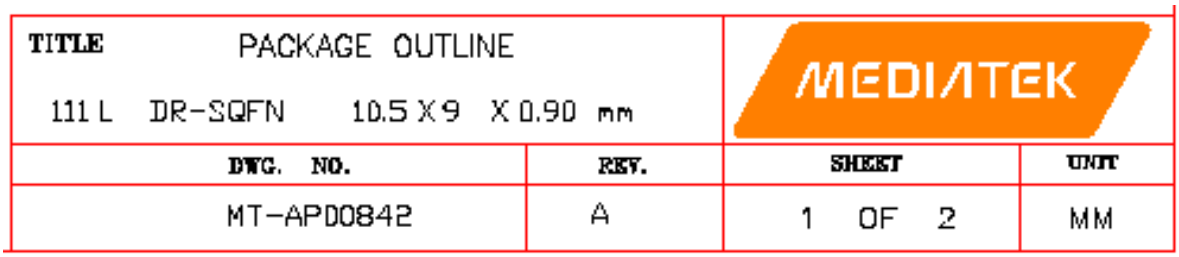


Figure 5-2. Physical dimension of MT7975DN

5.2 Ordering Information

Order No.	Marking	Temperature range	Package
MT7975DN	MT7975DN	-10°C ~ 70°C	DRQFN

ESD CAUTION

MT7975DN is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7975DN is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.